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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/22/2003

Valery M. Dubin

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10/06/2005

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EXAMINER

IM, JUNGHWA M

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/668,986

Applicant(s)

DUBIN ET AL.

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 May 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14, 32 and 33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 32 and 33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/10/2005.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 224, 2005 has been entered.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sambucetti et al. (US 6335104), hereinafter Sambucetti.

Regarding claim 1, Fig. 2 of Sambucetti shows an apparatus, comprising:

a semiconductor substrate (a region below the element 12);

a first conducting layer (12) in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu (col. 5, line 61-64);

a diffusion barrier (16) in contact with the first conducting layer;

a wetting layer (18) on top of the diffusion barrier; and

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a bump layer (40) on top of the wetting layer, the bump layer comprising Sn wherein the bump layer is an electroplated (col. 7, lines 55-59), and wherein the diffusion barrier being formed configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus.

It is noted that it is inherent that the diffusion barrier layer of Sambucetti's device is configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus since the material for the diffusion barrier layer of Sambucetti's device is identical to the one in the instant invention. Furthermore, it is known in the art that diffusion barrier layer is formed to prevent the intermetallic formation between the layers as disclosed by Sambucetti (col. 1, lines 39-41).

Regarding claim 2, it is inherent that the diffusion barrier layer of Sambucetti's device is configured to suppress whisker-type formation in the bump layer since the material for the diffusion barrier layer of Sambucetti's device is identical to the one in the instant invention. Furthermore, Sambucetti discloses that the diffusion barrier is utilized to alleviate whisker-type formation (lift-off defect; col. 1, lines 39-50).

Regarding claim 7, Fig. 2 of Sambucetti shows the wetting layer comprises NiP, (col. 6, lines 29-30) wherein the diffusion barrier is further configured to reduce bump layer delamination (lift-off defect; col. 1, lines 39-50).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (US 6827252), hereinafter Tong.

Regarding claim 1, Fig. 7 of Tong shows an apparatus, comprising:

a semiconductor substrate (310);

a first conducting layer (316, 320) in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu (col. 6, line 4);

a diffusion barrier (330) in contact with the first conducting layer;

a wetting layer (340) on top of the diffusion barrier; and

a bump layer (350) on top of the wetting layer, the bump layer comprising Sn (col. 4, lines 55-59), the Sn bump a layer, the diffusion barrier being formed configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus (col. 6, lines 43-46).

Also, note that "being electroplated" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 3, Fig. 14 of Tong shows a solder layer (380) positioned between the bump layer (370) and a die package, wherein the solder layer comprises Sn (col. 5, lines 4-7).

Regarding claim 8, Fig. 7 of Tong shows the apparatus further comprises an another base layer metal (320).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong in view of Mikagi et al. (US Pat. Pub. 2003/0025202), hereinafter Mikagi.

Regarding claim 4, Fig. 7 of Tong shows that the base layer metal comprises a Ti adhesion layer (320; col. 2, lines 58-61), however, fails to shows a seed layer comprised of one of Ni, NiV and Co. Fig. 14 of Mikagi shows a base metal layer comprising a Ti/TiN adhesion layer (13A, 13B), a NiV layer (32), and a Al/Cu layer (12). Note that a Ni-V layer can be formed of four layers shown in Fig. 5B, and one (161) of four layers can be a seed layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mikagi into the device of Tong in order to have a seed layer comprised of one of Ni, NiV and Co to improve the adhesion of the conductive layer to the substrate.

Regarding claim 5, Fig. 14 of Mikagi shows the base metal layer further comprises a metal layer (12) positioned between the adhesion layer and the NiV layer (32), wherein the metal layer comprises Al.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sambucetti in view of Tong.

Regarding claim 6, Fig. 2 of Sambucetti shows the diffusion barrier comprises one of NiBP, NiWP, NiWB, and NIWBP (col. 6, lines 1-2) however, fails to show “wherein the bump layer comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu,Bi, Sb, and 3.5Ag, wherein the Sn bump layer being electroplated is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn” Fig. 7 of Tong shows that the bump layer comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu,Bi, Sb, and 3.5Ag, wherein the Sn bump layer being electroplated is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn (col. 4, lines 54-59),

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tong into the device of Sambucetti in order to have the bump layer comprising a Sn alloy, the Sn alloy comprising one of 0.7Cu,Bi, Sb, and 3.5Ag, wherein the Sn bump layer being electroplated is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn to strengthen the connection of the solder bump to the package.

It is noted that it is well known in the art that the transformation of alpha Sn into beta Sn at low temperature.

Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong in view of Jin et al. (US 6740577), hereinafter Jin.

Regarding claims 9 and 13, Fig. 7 of Tong shows an apparatus, comprising:

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a base layer metal (316, 320) on a semiconductor substrate (310), the base layer metal comprising Cu (col. 6, line 4);

a bump layer (350) on top of the base layer metal;

a diffusion barrier (330) in contact with the bump layer;

a wetting layer (340) on top of the diffusion barrier; and

a solder layer (380) contacting the bump layer, the solder layer comprising Sn (col. 5, lines 4-7), the diffusion barrier being further configured to prevent the diffusion of Cu and Sn through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus (col. 6, lines 43-46), wherein the base metal layer further diffusion contacts the diffusion barrier layer to physically isolate the base metal layer and the bump.

Fig. 7 of Tong shows the most aspect of the instant invention except “the bump layer comprising an electroplated Cu layer.” Fig. 5 of Jin discloses a bump (16) formation through electroplating a Cu layer (28)

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Jin into the device of Tong in order to have a bump comprised of an electroplated Cu to improve the reliability of the connection between the bump and the package.

Claims 10 and 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tong and Jin as applied to claim 9 above, and further in view of Sambucetti.

Regarding claim 10, the combined teachings of Tong and Jin fail to show that the diffusion barrier layer is configured to suppress whisker-type formation in the bump layer.



Sambucetti's device discloses that the diffusion barrier layer is configured to suppress whisker-type formation in the bump layer (lift-off defect; col. 1, lines 39-50)..

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Sambucetti into the device of Tong and Jin in order to have the diffusion barrier configured to suppress whisker-type formation in the bump layer for a better connection of the bump to the package.

Regarding claim 14, Sambucetti discloses that the diffusion barrier comprises one of NiBP, NiWP, NiWB, and NiWBP, wherein the wetting layer comprises one of CoB and NiP. (col. 6, lines 1-30).

Claim 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong and Jin as applied to claim 9 above, and further in view of Mikagi.

Regarding claim 11, the combined teachings of Tong and Jin show that the base layer metal comprises a Ti adhesion layer (320; col. 2, lines 58-61), however, fails to shows a seed layer. Fig. 14 of Mikagi shows a base metal layer comprising a Ti/TiN adhesion layer (13A, 13B), a NiV layer (32), and a Al/Cu layer (12). Note that a Ni-V layer can be formed of four layers shown in Fig. 5B, and one (161) of four layers can be a seed layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mikagi into the device of Tong and Jin in order to have a seed layer to improve the adhesion of the conductive layer to the substrate.

Regarding claim 12, Fig. 14 of Mikagi shows the base metal layer further comprises a metal layer (12) positioned between the adhesion layer and the NiV layer (32), wherein the metal

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layer comprises Al. And it is obvious that the diffusion barrier layer of Tong is configured to suppress a whisker-type formation in the bump through preventing formation of SnCu intermetallic compounds.

Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong in view of Kazama et al. (US 6639315), hereinafter Kazama.

Regarding claim 32, Fig. 7 of Tong shows an apparatus, comprising:

a semiconductor substrate (310);

a first conducting layer (316, 320) in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu (col. 6, line 4);

a diffusion barrier (330) in contact with the first conducting layer;

a wetting layer (340) on top of the diffusion barrier; and

a bump layer (370) on top of the wetting layer, the bump layer comprising Sn, the Sn bump layer, the diffusion barrier being configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the die packaging interconnection (col. 6, lines 43-46).

Fig. 7 of Tong shows the most aspect of the instant invention except “one or more components comprising circuitry; and one and more layers on the circuit board to route at least one signal between components on the circuit board, wherein at least one of the components on the circuit board comprises a die packaging interconnect.” Fig. 5 of Kazama shows a circuit board (10) with a circuit for routing the signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kazama into the device of Tong in order to have a circuit board soldered to the interconnection of the semiconductor device to make a complete package.

Regarding claim 33, Kazama discloses a memory system on the circuit board (col. 15, line 18).

### *Response to Arguments*

Applicant's arguments with respect to claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection. However, Applicant's arguments regarding claims 13 and 32 have been fully considered but they are not persuasive.

Applicant mainly argues that "Tong fails to disclose that the diffusion barrier layer is configured to prevent Cu and Sn from diffusing through the diffusion barrier. In contrast, Tong discloses that the diffusion barrier layer itself can include Cu." It is pointed out that Tong discloses that the barrier layer can be made from one of the material such as nickel-vanadium alloy, chromium-copper alloy or nickel. (column 4, lines 3-5), therefore clearly indicating that the diffusion barrier layer can be made from the material other than Cu. Therefore, non-copper (Cu) layer forming the diffusion barrier layer of Tong is configured to prevent Cu and Sn from diffusing through the diffusion barrier layer and to prevent the intermetallic formation in the apparatus.

In response to Applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on

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obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. In re McLaughlin, 443 F.2d 1392; 170 USPQ 209 (CCPA 1971).

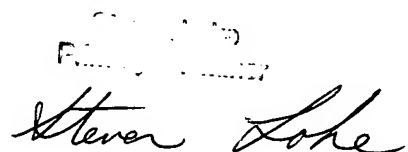
### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

  
Stephen Loke